What is claimed is:

1. A circuit comprising:

a first transistor;

a second transistor;

a ballast resistor coupled between an emitter terminal of the first transistor and a base terminal of the second transistor; and,

a feedback stabilization circuit coupled to the first transistor,

wherein a control voltage applied to a base terminal of the first transistor controls the amplification of a signal applied to the base terminal of the second transistor.

2. The circuit of claim 1, further comprising a biasing resistor coupled between a first input node and the base terminal of the first transistor.

3. The circuit of claim 1, wherein said feedback stabilization circuit includes at least one capacitor and at least one resistor.

4. The circuit of claim 1, further comprising a diode stack circuit coupled to the first transistor, said diode stack circuit including at least two transistors.

5. The circuit of claim 4, further comprising at least one bypass capacitor coupled to the at least two transistors.

6. The circuit of claim 1, further comprising at least one bypass capacitor coupled to the first transistor.

7. The circuit of claim 1, further comprising at least one additional resistor coupled between the emitter terminal of the first transistor and a base terminal of the first transistor.

8. A circuit comprising:

a first transistor;

a second transistor;

a ballast resistor coupled between an emitter terminal of the first transistor and a base terminal of the second transistor; and,

a diode stack circuit coupled to the first transistor,

wherein a control voltage applied to a base terminal of the first transistor controls the amplification of a signal applied to the base terminal of the second transistor.

9. The circuit of claim 8, further comprising a biasing resistor coupled between a first input node and the base terminal of the first transistor.

10. The circuit of claim 8, further comprising a feedback stabilization circuit, said feedback stabilization circuit including at least one capacitor and at least one resistor.

11. The circuit of claim 8, wherein the diode stack circuit includes at least two transistors.

12. The circuit of claim 11, further comprising at least one bypass capacitor coupled to the at least two transistors.

13. The circuit of claim 8, further comprising at least one bypass capacitor coupled to the first transistor.

14. The circuit of claim 8, further comprising at least one additional resistor coupled between the emitter terminal of the first transistor and a base terminal of the first transistor.

15. A circuit comprising:

a first transistor;

a second transistor;

a ballast resistor coupled between an emitter terminal of the first transistor and a base terminal of the second transistor; and,

at least one bypass capacitor coupled to a collector terminal of the first transistor,

wherein a control voltage applied to a base terminal of the first transistor controls the amplification of a signal applied to the base terminal of the second transistor.

16. The circuit of claim 15, further comprising a biasing resistor coupled between a first input node and the base terminal of the first transistor.

17. The circuit of claim 15, further comprising a feedback stabilization circuit, said feedback stabilization circuit including at least one capacitor and at least one resistor.

18. The circuit of claim 15, further comprising a diode stack circuit, wherein the diode stack circuit includes at least two transistors.

19. The circuit of claim 18, further comprising at least one bypass capacitor coupled to the at least two transistors.

20. The circuit of claim 15, further comprising at least one additional resistor coupled between the emitter terminal of the first transistor and a base terminal of the first transistor.

21. A circuit comprising:

a first transistor;

a second transistor;

a ballast resistor coupled between an emitter terminal of the first transistor and a base terminal of the second transistor; and,

at least one additional resistor coupled between the emitter terminal of the first transistor and a base terminal of the first transistor,

wherein a control voltage applied to a base terminal of the first transistor controls the amplification of a signal applied to the base terminal of the second transistor.

22. The circuit of claim 21, further comprising a biasing resistor coupled between a first input node and the base terminal of the first transistor.

23. The circuit of claim 21, further comprising a feedback stabilization circuit, wherein said feedback stabilization circuit includes at least one capacitor and at least one resistor.

24. The circuit of claim 21, further comprising a diode stack circuit coupled to the first transistor, said diode stack circuit including at least two transistors.

25. The circuit of claim 24, further comprising at least one bypass capacitor coupled to the at least two transistors.

26. The circuit of claim 21, further comprising at least one bypass capacitor coupled to the first transistor.

27. A method for amplifying a signal, comprising the steps of:

providing a control signal to a base terminal of a first transistor;

creating a bias voltage across a ballast resistor coupled to an emitter terminal of the first transistor;

providing feedback stabilization of the control signal; and,

applying the bias voltage to the base terminal of a second transistor to change the amplification of a signal also applied to the base terminal of the second transistor.

28. A method for amplifying a signal, comprising the steps of:

providing a control signal to a base terminal of a first transistor;

creating a bias voltage across a ballast resistor coupled to an emitter terminal of the first transistor;

providing a circuit to compensate for temperature variations; and,

applying the bias voltage to the base terminal of a second transistor to change the amplification of a signal also applied to the base terminal of the second transistor.

29. A method for amplifying a signal, comprising the steps of:

providing a control signal to a base terminal of a first transistor;

creating a bias voltage across a ballast resistor coupled to an emitter terminal of the first transistor;

providing at least one bypass capacitor coupled to a collector terminal of the first transistor to improve peak operating performance; and,

applying the bias voltage to the base terminal of a second transistor to change the amplification of a signal also applied to the base terminal of the second transistor.

30. A method for amplifying a signal, comprising the steps of:

providing a control signal to a base terminal of a first transistor;

creating a bias voltage across a ballast resistor coupled to an emitter terminal of the first transistor;

providing at least one resistor coupled between the base terminal and the emitter terminal of the first transistor to reduce the power control waveform slope; and,

applying the bias voltage to the base terminal of a second transistor to change the amplification of a signal also applied to the base terminal of the second transistor.